

[Close] [Minimize] [Maximize] [Close]

- ↪ L31: (2464) single near2 anchor \$4
- ↪ L32: (36) 17 near5 31
- ↪ L33: (2) *6551916*.pn.
- ↪ L34: (1) Forward citation search 1
- ↪ L35: (4) Backward citation search 1
- ↪ L36: (5) 29 33
- ↪ L37: (1) Forward citation search 2
- ↪ L38: (4) Backward citation search 2
- ↪ L39: (1) Forward citation search 3
- ↪ L40: (5) Backward citation search 3
- ↪ L41: (1) Forward citation search 4
- ↪ L42: (7) Backward citation search 4
- ↪ L43: (0) Forward citation search 5
- ↪ L44: (4) Backward citation search 5
- ↪ L45: (1) Forward citation search 6
- ↪ L46: (6) Backward citation search 6
- ↪ L47: (2) Forward citation search 7
- ↪ L48: (2) Forward citation search 8
- ↪ L49: (4886)(257/700,703,758).CCLS
- ↪ L50: (1) 31 and 49
- ↪ L51: (197) 49 and 18
- ↪ L52: (4) 51 and 28
- ↪ L53: (4973) 28 and 17
- ↪ L54: (1238) 28 same 17
- ↪ L55: (67) 54 and 48

Failed

DBs: US-PGPUB, USPAT, EPO, IPO, DERWENT, IBM, TD8
 Plurals

Default operator: OR
 Highlight all hit terms initially

54 and 49

GRS form ISRP form Image Text HTML

U	I	Investor	Document/Issue#	P	Title	Current	Current	XRef	Retrieval	S	C	P	Y	Image	Date	P
1	<input type="checkbox"/>	Palmer, Willi	US 2004020 20041	I	Through-via vertical interconnects, through-via	257/700	257/698			<input type="checkbox"/>	US 200402					
2	<input type="checkbox"/>	Meguro, Hisa	US 2004014 20040	I	Semiconductor memory device	257/776	257/752			<input type="checkbox"/>	US 200401					
3	<input type="checkbox"/>	Matsunaga, T	US 2004013 20040	I	Semiconductor device and its manufacturing	257/758				<input type="checkbox"/>	US 200401					
4	<input type="checkbox"/>	Fukuda, Yuta	US 2004008 20040	I	Semiconductor equipment	257/758	257/E23.01			<input type="checkbox"/>	US 200400					
5	<input type="checkbox"/>	Teh, Young	US 2004006 20040	I	Novel copper metal structure for the reducti	257/751	257/759			<input type="checkbox"/>	US 200400					
6	<input type="checkbox"/>	Avanai, Kats	US 2003023 20031	I	Memory device and method of production an	257/758	257/E27.00			<input type="checkbox"/>	US 200302					
7	<input type="checkbox"/>	Saitoh, Yumi	US 2003020 20031	I	METHOD OF FORMING A MULTI-LAYERED W	257/758	257/E23.14			<input type="checkbox"/>	US 200302					
8	<input type="checkbox"/>	Dennison, Ch	US 2003009 20030	I	Semiconductor processing methods of formin	257/758	257/774			<input type="checkbox"/>	US 200300					
9	<input type="checkbox"/>	Cho, Tai-Huei	US 2002018 20021	I	Semiconductor device having multilevel inter	257/758	257/E23.14			<input type="checkbox"/>	US 200201					
10	<input type="checkbox"/>	Teh, Young	US 2002017 20021	I	Novel copper metal structure for the reducti	257/751	257/700			<input type="checkbox"/>	US 200201					

File Details HTML

Ready

304M